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The claims have been amended as follows:

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6. (Amended) <u>An apparatus</u> [A computer system] comprising: an interface adapted to:

receive a request from <u>a</u> [another] computer system for identification of the <u>apparatus</u> [first computer system], and

furnish a hash value that identifies the <u>apparatus</u> [first computer system] to <u>the</u> [said another] computer system; and

a processor coupled to the interface and adapted to:

encrypt an identifier that identifies the <u>apparatus</u> [first computer system] with a key associated with <u>the</u> [said another] computer system to produce the hash value.

- 7. (Amended) The <u>apparatus</u> [computer system] of claim 6, wherein the identifier comprises a processor number that identifies the processor.
- 8. (Amended) The <u>apparatus</u> [computer system] of claim 6, wherein the processor comprises:

a memory adapted to store microcode for performing the encryption; and a control unit coupled to the memory and adapted to execute the microcode to perform the encryption.

9. (Amended) The <u>apparatus</u> [computer system] of claim 6, wherein the processor is further adapted to:

interact with the interface to receive the key from the [said another] computer system.

16. (Amended) The microprocessor of claim 15, wherein the execution unit comprises:

a control unit [coupled to the algorithmic unit and the registers]; and

a memory coupled to the control unit and storing microcode to cause the control unit to use the key and the identifier to produce the hash value.